AMENDMENTS TO THE SPECIFICATION

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Figures 5A – 5[[F]]E are schematic cross-sectional views illustrating the steps in one embodiment of a process for fabricating a NAND flash memory cell array in accordance with the invention.

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The control gates are fabricated of a conductive material such as a doped polysilicon or polycide, and [[is]] are insulated from the floating gates beneath them by dielectric films 42. Those films can be either a pure oxide or a combination of oxide, nitride and oxide (ONO), and in one presently preferred embodiment, they consist of a layer nitride between two layers of oxide.

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Thereafter, a glass material 60 such as phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG) is deposited across the entire wafer, then etched to form openings for bit line contacts 46~~, as shown in Figure 5F~~. Finally, a metal layer is deposited over the glass and patterned to form bit lines 57 and bit line contacts 46, as shown in Figure 3.